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EXAMINER

HUBER, ROBERT T

ART UNIT	PAPER NUMBER
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2892

NOTIFICATION DATE	DELIVERY MODE
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ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/582,035	Applicant(s) SHEN ET AL.	
	Examiner ROBERT HUBER	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 May 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 June 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>05/28/2008</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to because the drawings have unclear, hand-numbered reference numbers. Also, the examiner requests the Applicant to review the reference characters and numbering of the drain, gates, and sources of the transistors shown in figure 4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 6, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Perugupalli et al. (US 6,455,905 B1).

a. Regarding claim 1, **Perugupalli discloses a monolithic structure** (e.g. figure 11, and clarified in the figure below), **comprising:**

a first pair of devices (devices 1 and 2, as seen in the figure below) **and a second pair of devices** (devices 3 and 4, as seen in the figure below), **each pair of devices comprising:**

a first lateral device having a first source terminal, a first drain terminal, and a first gate terminal (e.g. first lateral devices 1 and 3 each have a source, drain, and gate terminal, and are lateral, as seen in the figure below and clarified in figures 4, 6, and 9 of Perugupalli), **each of said first source, first drain, and first gate terminals terminating on a first surface of a semiconductor substrate** (e.g. as seen the figure below and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320);

and a second lateral device having a second source terminal, a second drain terminal, and a second gate terminal (e.g. second lateral

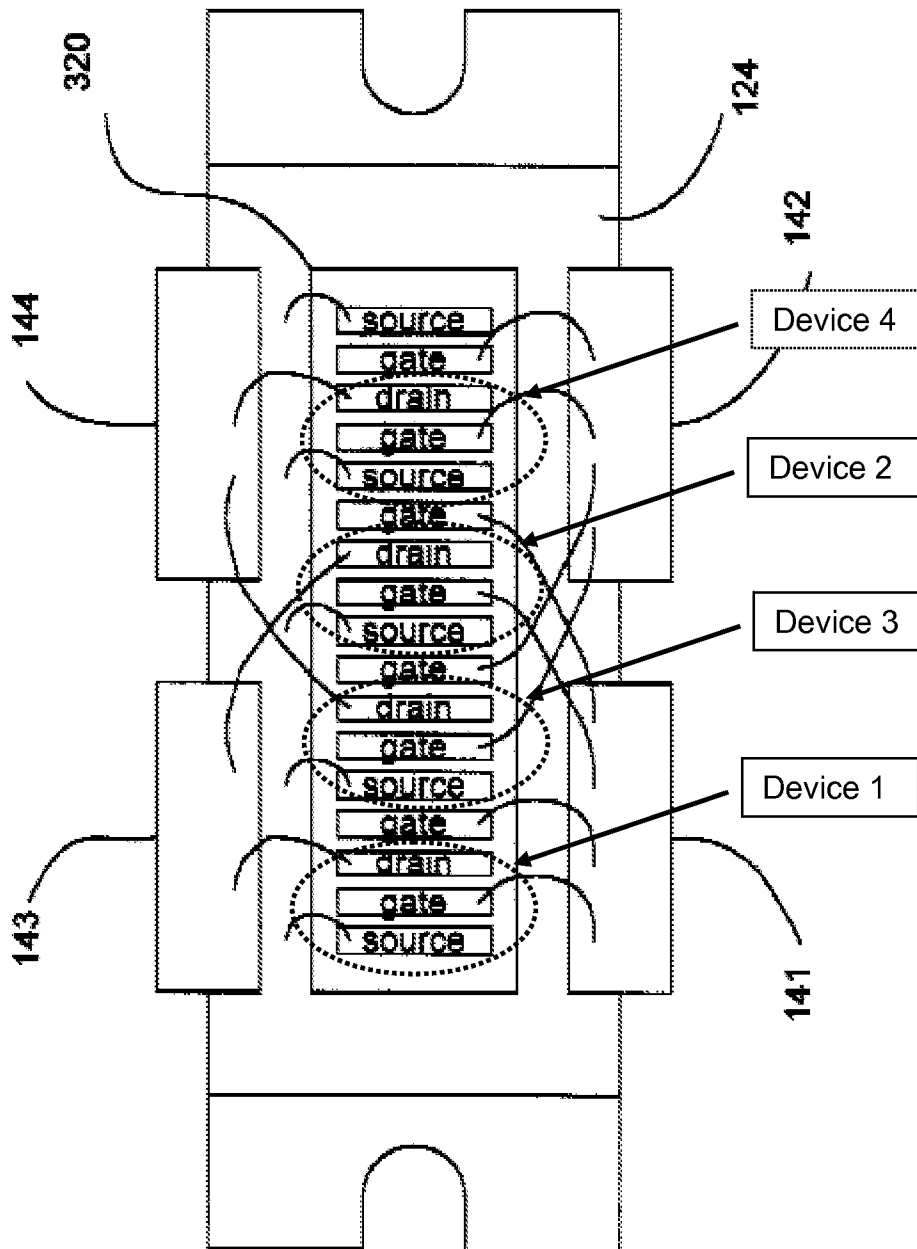
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devices 2 and 4 each have a source, drain, and gate terminal, and are lateral, as seen in the figure below and clarified in figures 4, 6, and 9 of Perugupalli), **each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate** (e.g. as seen the figure below and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320),

said first drain terminal being connected to said second drain terminal (e.g. as seen in the figure below, first drain terminal of device 1 is connected to second drain terminal of device 2 via the drain lead 143, and first drain terminal of device 3 is connected to second drain terminal of device 2 via the drain lead 144), **and said first gate terminal being connected to second to said second gate terminal** (e.g. first gate terminal of device 1 is connected to second gate terminal of device 2 via gate lead 141, and first gate terminal of device 3 is connected to second gate terminal of device 4 via gate lead 142),

wherein (i) in each pair of devices, each first lateral device is combined with each second lateral device on said substrate (e.g. as seen in figure 11), **(ii) both first source terminals are connected to both second source terminals to define a common source terminal of the monolithic structure** (e.g. as seen in the figure, both first source terminals are connected to both second source terminals via common source terminal 124), **and (iii) a first electrically isolated lead comprises the common source terminal** (source

terminals are connect to each other via wire bonding to the isolated lead 124, as seen in figure 11 and disclosed in col. 5, lines 14 – 19).



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b. Regarding claim 3, **Perugupalli discloses the monolithic structure of claim 1, as cited above, wherein said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of devices** (e.g. as seen in the figure above, first and second drain terminals of the first pair of devices, 1 and 2, are connected to drain lead 143, while first and second drain terminals of the second pair of devices, 3 and 4, are connected to drain lead 144. Therefore, they are independent).

c. Regarding claim 4, **Perugupalli discloses the monolithic structure of claim 3, as cited above, wherein said first and second gate terminals of the first pair of devices are electrically independent of the first and second gate terminals of the second pair of devices** (e.g. as seen in the figure above, first and second gate terminals of the first pair of devices, 1 and 2, are connected to gate lead 141, while first and second gate terminals of the second pair of devices, 3 and 4, are connected to gate lead 142. Therefore, they are independent).

d. Regarding claim 6, **Perugupalli discloses the monolithic structure of claim 1, wherein each of said first and second lateral devices comprises a lateral power MOSFET** (e.g. col. 3, line 60 discloses the transistors to be

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LDMOS transistors, and col. 1, lines 14 - 16 disclose that LDMOS (laterally diffused MOSFET) transistor may be used for power applications).

e. Regarding claim 13, **Perugupalli discloses a monolithic structure comprising at least for lateral power transistor devices combined on a semiconductor substrate** (e.g. figure 11, and clarified in the figure above), **said structure comprising:**

a first pair of power transistor devices (power transistor devices 1 and 2, as seen in the figure above) **and a second pair of power transistor devices** (power transistor devices 3 and 4, as seen in the figure above), **each pair of power transistor devices comprising:**

a first lateral power transistor device comprising a first source terminal, a first drain terminal, and a first gate terminal (e.g. first lateral devices 1 and 3 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320);

a second lateral power transistor device having a second source terminal, a second drain terminal, and a second gate terminal (e.g. second lateral power transistor devices 2 and 4 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6,

and 9 of Perugupalli), **said second source, second drain, and second gate terminals terminating on said first surface** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320),

said first drain terminal being connected to said second drain terminal (e.g. as seen in the figure above, first drain terminal of device 1 is connected to second drain terminal of device 2 via the drain lead 143, and first drain terminal of device 3 is connected to second drain terminal of device 2 via the drain lead 144), **and said first gate terminal being connected to said second gate terminal** (e.g. first gate terminal of device 1 is connected to second gate terminal of device 2 via gate lead 141, and first gate terminal of device 3 is connected to second gate terminal of device 4 via gate lead 142),

wherein (i) said first and second gate terminals of the first pair of power transistor devices are electrically independent of the first and second gate terminals of the second pair of power transistor devices (e.g. as seen in the figure above, first and second gate terminals of the first pair of devices, 1 and 2, are connected to gate lead 141, while first and second gate terminals of the second pair of devices, 3 and 4, are connected to gate lead 142. Therefore, they are independent);

(ii) said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of devices (e.g. as seen in the figure above, first and second drain

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terminals of the first pair of devices, 1 and 2, are connected to drain lead 143, while first and second drain terminals of the second pair of devices, 3 and 4, are connected to drain lead 144. Therefore, they are independent),

(iii) a first electrically isolated lead comprises both first source terminals connected to both second source terminals (e.g. as seen in the figure above, both first source terminals are connect to both second source terminals via common source terminal 124),

(iv) a second electrically isolated lead comprises said first and second drain terminals of the second pair of power transistor devices (lead 143),

(v) a third electrically isolated lead comprises said first and second drain terminals of the second pair of power transistor devices (lead 144);

(vi) a fourth electrically isolated lead comprises said first and second gate terminals of the first pair of power transistor devices (lead 141), and

(vii) a fifth electrically isolated lead comprising said first and second gate terminals of the second pair of power transistor devices (lead 142).

f. Regarding claim 14, **Perugupalli discloses the monolithic structure of claim 13, as cited above, wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET** (e.g. col. 3, line 60 discloses the transistors to be LDMOS transistors, and col. 1, lines 14 - 16

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disclose that LDMOS (laterally diffused MOSFET) transistors may be used for power applications).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli in view of Forbes (US 2002/0008549 A1).

a. Regarding claim 5, **Perugupalli discloses the monolithic structure of claim 3, as cited above, but is silent with respect to wherein said first and second gate terminals of the first pair of devices are connected to said first**

and second drain terminals of the second pair of devices and said first and second gate terminals of the second pair of devices are connected to said first and second drain terminals of the first pair of devices.

Forbes discloses a circuit device (e.g. figure 4) **wherein first and second gate terminals of the first pair of devices** (first and second gate terminals 418A and 409A of first pair of devices Q3 and Q1, respectively) **are connected to first and second drain terminals of the second pair of devices** (as seen in the figure, first and second gate terminals of the first pair of devices are connected to the first and second drain terminals at point 424B of the second pair of devices Q4 and Q2), **and first and second gate terminals of the second pair of devices** (first and second gate terminals 418B and 409B of second pair of devices Q4 and Q2, respectively) **are connected to said first and second drain terminals of the first pair of devices** (as seen in the figure, first and second gate terminals of the second pair of devices are connected to the first and second drain terminals at point 424A of the first pair of devices Q3 and Q1).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Perugupalli such that the first and second gate terminals of the first pair of devices were connected to the first and second drain of the second pair of devices, and vice versa, since Perugupalli discloses a structure comprising a set of push-pull transistors in a monolithic structure, and Forbes discloses that a set of push-pull transistors may be

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connected in such a manner as described. One would have been motivated to connect the drains and gates of the pairs of transistors as described in order to produce a differential amplifier circuit (as described by Forbes, ¶ [0028]) on a single substrate.

b. Regarding claim 7, **Perugupalli discloses a monolithic structure comprising at least four lateral power transistor devices combined on a semiconductor substrate** (e.g. figure 11, and clarified in the figure above), **said monolithic structure comprising:**

a first pair of power transistor devices (power transistor devices 1 and 2, as seen in the figure above) **and a second pair of power transistor devices** (power transistor devices 3 and 4, as seen in the figure above), **each pair of transistor devices comprising:**

a first lateral power transistor device comprising a first source terminal, a first drain terminal, and a first gate terminal (e.g. first lateral devices 1 and 3 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **each of said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320);

a second lateral power transistor device comprising a second source terminal, a second drain terminal, and a second gate terminal (e.g. second lateral power transistor devices 2 and 4 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320),

said first drain terminal being connected to said second drain terminal (e.g. as seen in the figure above, first drain terminal of device 1 is connected to second drain terminal of device 2 via the drain lead 143, and first drain terminal of device 3 is connected to second drain terminal of device 2 via the drain lead 144), **and said first gate terminal being connected to said second gate terminal** (e.g. first gate terminal of device 1 is connected to second gate terminal of device 2 via gate lead 141, and first gate terminal of device 3 is connected to second gate terminal of device 4 via gate lead 142),

(iii) said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of power transistor devices (e.g. as seen in the figure above, first and second drain terminals of the first pair of devices, 1 and 2, are connected to drain lead 143, while first and second drain terminals of the second pair of

devices, 3 and 4, are connected to drain lead 144. Therefore, they are independent),

(iv) a first electrically isolated lead comprises both first source terminals connected to both second source terminals (e.g. as seen in the figure above, both first source terminals are connect to both second source terminals via common source terminal 124),

(v) a second electrically isolated lead comprises said first and second drain terminals of the first pair of power transistor devices (lead 143), and

(vi) a third electrically isolated lead comprises said second drain terminals of the second pair of transistor devices (lead 144).

Perugupalli is silent with respect to wherein (i) said first and second gate terminals of the first pair of power transistor devices are connected to said first and second drain terminals of the second pair of power transistor devices, and (ii) said first and second gate terminals of the second pair of devices are connected to said first and second drain terminals of the first pair of power transistor devices.

Forbes discloses a circuit device (e.g. figure 4) wherein first and second gate terminals of the first pair of transistor devices (first and second gate terminals 418A and 409A of first pair of devices Q3 and Q1, respectively) are connected to first and second drain terminals of the second pair of transistor devices (as seen in the figure, first and second gate terminals of the

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first pair of devices are connected to the first and second drain terminals at point 424B of the second pair of devices Q4 and Q2), **and first and second gate terminals of the second pair of devices** (first and second gate terminals 418B and 409B of second pair of devices Q4 and Q2, respectively) **are connected to said first and second drain terminals of the first pair of devices** (as seen in the figure, first and second gate terminals of the second pair of devices are connected to the first and second drain terminals at point 424A of the first pair of devices Q3 and Q1).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Perugupalli such that the first and second gate terminals of the first pair of devices were connected to the first and second drain of the second pair of devices, and vice versa, since Perugupalli discloses a structure comprising a set of push-pull transistors in a monolithic structure, and Forbes discloses that a set of push-pull transistors may be connected in such a manner as described. One would have been motivated to connect the drains and gates of the pairs of transistors as described in order to produce a differential amplifier circuit (as described by Forbes, ¶ [0028]) on a single substrate.

c. Regarding claim 8, **Perugupalli in view of Forbes further disclose the monolithic structure of claim 7, wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET** (e.g.

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col. 3, line 60 discloses the transistors to be LDMOS transistors, and col. 1, lines 14 - 16 disclose that LDMOS (laterally diffused MOSFET) transistors may be used for power applications).

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli in view of Alder et al. (US 4,656,493).

a. Regarding claim 9, **Perugupalli discloses a monolithic structure comprising at least four lateral power transistor devices combined on a semiconductor substrate** (e.g. figure 11, and clarified in the figure above), **said monolithic structure comprising:**

a first pair of power transistor devices (power transistor devices 1 and 2, as seen in the figure above) **and a second pair of power transistor devices** (power transistor devices 3 and 4, as seen in the figure above), **each pair of transistor devices comprising:**

a first lateral power transistor device comprising a first source terminal, a first drain terminal, and a first gate terminal (e.g. first lateral devices 1 and 3 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **each of said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320);

a second lateral power transistor device comprising a second source terminal, a second drain terminal, and a second gate terminal (e.g. second lateral power transistor devices 2 and 4 each have a source, drain, and gate terminal, and are lateral, as seen in the figure above and clarified in figures 4, 6, and 9 of Perugupalli), **each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate** (e.g. as seen the figure above and clarified in figures 4, 6, and 9, and col. 5, lines 46 - 50 with respect to the chip 320),

said first drain terminal being connected to said second drain terminal (e.g. as seen in the figure above, first drain terminal of device 1 is connected to second drain terminal of device 2 via the drain lead 143, and first drain terminal of device 3 is connected to second drain terminal of device 2 via the drain lead 144), **and said first gate terminal being connected to said second gate terminal** (e.g. first gate terminal of device 1 is connected to second gate terminal of device 2 via gate lead 141, and first gate terminal of device 3 is connected to second gate terminal of device 4 via gate lead 142),

wherein (i) a first electrically isolated lead comprises both first source terminals connected to both second source terminals (e.g. as seen in the figure above, both first source terminals are connect to both second source terminals via common source terminal 124),

(ii) a second electrically isolated lead comprises said first and second drain terminals of the first pair of power transistor devices (lead 143),

(iii) a third electrically isolated lead comprises said first and second drain terminals of the second pair of power transistor devices (lead 144).

Perugupalli is silent with respect to (iii) a fourth electrically isolated lead comprises said first and second gate terminals of the first pair of power transistor devices connected to said first and second gate terminals of the second pair of power transistor devices.

Alder discloses a monolithic circuit device (e.g. figure 3) wherein a fourth electrically isolated lead (gate lead 88) comprises said first and second gate terminals of the first pair of power transistor devices (gate terminals 84 of the first pair of power transistor devices on the left side of the substrate) connected to said first and second gate terminals of the second pair of power transistor devices (gate terminals 86 of the second pair of power transistor devices on the right side of the substrate).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Perugupalli such that the first and second gate terminals of the first pair of devices were connected to the first and second gate terminals of the second pair of devices, since Perugupalli discloses a structure comprising a set of transistors in a monolithic structure, and Alder discloses that a set of transistors in a monolithic structure may be connected in

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such a manner as described. One would have been motivated to connect the gates of the pairs of transistors as described in order to produce a symmetrical bidirectional power MOSFET device (as described by Alder, col. 7, lines 38 – 40) on a single substrate.

b. Regarding claim 10, **Perugupalli in view of Alder further disclose the monolithic structure of claim 9, wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET** (e.g. col. 3, line 60 discloses the transistors to be LDMOS transistors, and col. 1, lines 14 - 16 disclose that LDMOS (laterally diffused MOSFET) transistors may be used for power applications).

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli in view of Alder as applied to claim 9 above, and further in view of Green (US 4,472,871).

a. Regarding claim 11, **Perugupalli in view of Alder disclose the monolithic structure of claim 9, but are silent with respect to the size of said second lateral power transistor being smaller than a size of said first lateral power transistor.**

Green teaches that for multiple transistors on the same substrate, the size of the second transistor may be smaller than the size of the first transistor (col. 4, lines 59 - 61).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli such that the second power transistor is smaller than the first, since it was known in the art to make transistors of different sizes in a monolithic structure, as disclosed by Green. One would be motivated to make such a modification since the electrical characteristics, such as the switching speed or current through the device can be affected by reducing dimension size.

b. Regarding claim 12, **Perugupalli in view of Alder disclose the monolithic structure of claim 9, but is silent with respect to a first threshold voltage of said first lateral power transistor being different from a second threshold voltage of said second lateral power transistors and a difference in said first and second threshold voltages is at least ranging approximately 0.1 V.**

Green teaches that for multiple transistors on the same substrate the threshold voltages may be different by up to 1.75 V (e.g. table in col. 3).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli such that the threshold voltages of the two power transistors of a monolithic structure differ by over 0.1 V, since Green teaches that such modifications are known in the art. One would be motivated to make such a modification in order to allow for

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more flexibility in circuit design, as well as for an increase in transistor switching speed, as disclosed in Green (col. 3, lines 52 - 53, and col. 4, lines 33 - 34).

9. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perugupalli in view of Green.

a. Regarding claim 15, **Perugupalli discloses the monolithic structure of claim 13, but is silent with respect to the size of said second lateral power transistor being smaller than a size of said first lateral power transistor.**

Green teaches that for multiple transistors on the same substrate, the size of the second transistor may be smaller than the size of the first transistor (col. 4, lines 59 - 61).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli such that the second power transistor is smaller than the first, since it was known in the art to make transistors of different sizes in a monolithic structure, as disclosed by Green. One would be motivated to make such a modification since the electrical characteristics, such as the switching speed or current through the device can be affected by reducing dimension size.

b. Regarding claim 16, **Perugupalli discloses the monolithic structure of claim 13, but is silent with respect to a first threshold voltage of said first lateral power transistor being different from a second threshold voltage of**

said second lateral power transistors and a difference in said first and second threshold voltages is at least ranging approximately 0.1 V.

Green teaches that for multiple transistors on the same substrate the threshold voltages may be different by up to 1.75 V (e.g. table in col. 3).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the monolithic structure of Perugupalli such that the threshold voltages of the two power transistors of a monolithic structure differ by over 0.1 V, since Green teaches that such modifications are known in the art. One would be motivated to make such a modification in order to allow for more flexibility in circuit design, as well as for an increase in transistor switching speed, as disclosed in Green (col. 3, lines 52 - 53, and col. 4, lines 33 - 34).

Response to Arguments

10. Applicant's arguments with respect to claims 1 and 13 have been considered but are moot in view of the new ground(s) of rejection. At present, the prior art of Perugupalli remains commensurate to the scope of the claims as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above. In response to Applicants arguments drawn to the amendment, *"a first and second pair of devices wherein both first source terminals are connected to both second source terminals, with each source terminal terminating on the first surface of a semiconductor substrate"*, Perugupalli shows (e.g. in figures 04, 06, and 08), that all of the terminals of the device

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do terminate on the first surface of the substrate 322, and that the chip 320 of figure 11 comprises the substrate 322. The sources, drains, and gates of the transistors are further connected through connections in a manner recited in the claims, as shown in figure 11. Therefore, the prior art of Perugupalli anticipates the claimed inventions recited in claims 1 and 13.

11. Applicant's arguments with respect to claims 7 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
August 15, 2008